Analysis of the Soft Error Susceptibility and Failure Rate in Logic Circuits

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Abstract: *The failure rate of logic circuits due to high-energy particles originating from outer space has been increasing dramatically over the past 10 years. Whereas soft errors have traditionally been of much greater concern in memories, smaller feature sizes, lower voltage levels, higher operating frequencies, and reduced logic depth are projected to cause a dramatic increase in soft error failure rate in core combinational logic in near-future technologies. Traditional fault tolerance strategies may be utilized to protect against these failures; however, the excessive area overhead and stringent power dissipation requirements have made these techniques obsolete, especially in mainstream applications. Therefore, there is an urgent necessity to identify the weak steps during the synthesis of these components that result in the generation of highly-susceptible designs. In this paper, we analyze the susceptibility of logic circuits to transient pulses through an extensive set of logic synthesis experiments while varying the synthesis process. Our aim is to identify the correlation between the key design options and their consequent effect on the susceptibility of the produced implementation. The results in this work reveal that the SER is strongly correlated with logical masking of transient pulses and, thus, fast logic-level soft error failure rate assessment methods can be used in place of computationally-intensive circuit-level assessment techniques. Furthermore, we project that logical masking will become the dominant source for protecting logic circuits from transient pulses, which encourages the development of logic synthesis techniques that maximize the logical masking of potential transient pulses.*

Keywords: *Single-event transient, soft errors, soft error susceptibility, soft error failure rate, and soft error sensitization probability.*

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1. Introduction

When high-energy neutrons or alpha particles strike a sensitive region in a semiconductor, they generate a transient pulse, commonly known as a Single-Event Transient (SET), in the form of an unexpected current pulse of a short duration. Under certain circumstances, the latter may be misinterpreted by the circuit as a valid signal and result in an incorrect output, thus producing a soft error. Such soft errors, which only distort the data processed by the circuit but make no damage to the hardware itself, are emerging as a serious threat to the reliable operation of logic circuits.

Historically, soft errors have been of great concern in memories and, as a result, various solutions to cope with soft errors in memories have been developed in the literature. Memories occupy a large area of silicon and comprise storage elements that are much more susceptible to particle strikes than combinational logic [15], SETs in which are frequently masked before reaching an output or a storage element [17]. However, technological trends such as faster clock rates, smaller device sizes, lower supply voltages, and shallower logic depths are drastically reducing SET masking and significantly increasing the occurrence of soft errors in combinational logic. Hence, the Soft Error failure Rate (SER) of logic circuits implemented using near-future CMOS technology is projected to surpass that of unprotected memory elements by the year 2011 [28].

To this end, various methods have been proposed in the literature [5, 6, 7, 11, 14, 19, 21, 25, 33, 34] to reduce the SER of a circuit and, thus, improve its reliability. The idea behind these methods revolves around developing solutions at the physical level, wherein individual transistor characteristics are perturbed to reduce the sensitivity of logic gates to SETs. While these methods are particularly effective in reducing the SER of a design, they are technology dependent, i.e., they rely on information available only after mapping of a circuit to a target technology. In contrast, in this work we evaluate technology-independent design choices, i.e., logic-level synthesis options that produce, among the many possible gate-level implementations of a circuit, the one that minimizes its SER. While such logic-level methods cannot benefit from the detailed information available at the physical level, and, thus, may not be able to provide comparable levels of SER reduction, they offer two unique advantages [1, 2, 3]. First, they enable design modifications for SER reduction that are equally effective independent of the technology to which the circuit will be mapped. Second, they provide the ability to consider SER as a design objective much earlier in the design cycle. Moreover,

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the mechanisms through which soft errors can be averted at the logic level are typically orthogonal to those at the physical level; hence, logic-level SER reduction methods do not intend to substitute their physical-level counterparts but, rather, to provide a better starting point.

In this paper, we study the increased susceptibility of logic circuits to transient errors. We perform an extensive set of experiments while varying the synthesis process, in order to reveal the correlation between the design synthesis options and their consequent effect on the susceptibility of the produced implementation. The key findings of our study can aid design engineers to identify the susceptibility of the implementation early in the design cycle, which enables the incorporation of additional resources for soft error protection when needed. The results of this study indicate that the SER is strongly correlated with logical masking of transient pulses, and that it will become the dominant source for protecting logic circuits from transient pulses in future technologies. Hence, our results encourage the development of synthesis-for-reliability techniques for logic circuits, which produce an error-resilient realization of a logic function by maximizing the internal logical masking of potential transient pulses.

The outline of the paper is as follows. First, in section 2, we review the prior work in the area of soft error modeling and SER reduction in logic circuits. Next, in section 3, we describe how transient pulses may produce soft errors in logic circuits, and the current design practices that increase the susceptibility of combinational logic to soft errors. In section 4, we perform an extensive set of experiments to analyze the susceptibility of logic circuits produced under various logic synthesis options. Finally, the conclusions are summarized in section 5.

2. Prior Work

The SER of a combinational circuit is proportional to three factors [28]: the rate of SET occurrence at a logic gate (R_{SET}), the probability of a SET arriving at a storage element during its latching window (P_{latch}), and the probability of a SET propagating to an output through a sensitized path (P_{sens}). In order to reduce the SER of a circuit, previous soft error mitigation methods have focused on one of these factors.

Soft error rate reduction via R_{SET} reduction is based on circuit-level design modifications, wherein individual transistor characteristics are perturbed to reduce the sensitivity of logic gates to SETs. Specifically, such methods resize the (W)idth/(L)ength ratios of the transistors in a select set of gates, in order to increase their immunity to SETs and, by extension, reduce R_{SET} and the SER of the circuit. SER estimation and assessment of gate susceptibility to soft errors is performed either through fault injection and simulation, wherein the SET masking factors are evaluated separately [22, 31, 33], or through symbolic representation, wherein all SET masking factors are evaluated in a unified approach [14, 20, 32]. In either way, gate resizing is performed for the most susceptible logic gates, i.e., the ones that contribute the most to the SER of the design [6, 19, 34].

Soft error rate reduction via P_{latch} reduction is based on redesigning the storage elements of the circuit in order to prevent latching of SETs occurring in Flip-Flops (FFs) [23, 26], combinational logic [8, 10, 24], or both [9, 18, 21]. Such methods take advantage of the temporal nature of SETs and tolerate them via fine-grained time redundancy [8, 10, 24]. In this case, the flip-flop inputs are sampled multiple times within the slack time available for each output of the circuit, and a majority voter selects the winner of the sampled values, which is, subsequently, stored in each flip-flop. This reduces the SET latching window and, by extension, the P_{latch} and the SER of the circuit. In an effort to reduce the incurred cost, several methods that utilize existing test and debug system resources to implement time redundancy-based soft error mitigation have been recently proposed [9, 21].

In contrast to these circuit-level solutions, soft error rate reduction via P_{sens} reduction mitigates soft errors at the logic level. In [1], a set of functionally redundant wires that realize logic implications between internal signal values is added to the circuit. Logical implications can be identified by using learning techniques such as backward justification, direct implications, or indirect implications, each capturing a subset of the existing implications in different computational complexities. Once the implications are identified, their addition as wires reduces the probability of SETs reaching a primary output of the circuit and, by extension, its SER. In [12, 13], logic rewriting is used to identify functionally-equivalent replacement candidates for a small sub-circuit in the original design. The target sub-circuit is selected based on its sensitivity to transient pulses, as well as the number of transient pulses that may propagate through the sub-circuit. Once the most susceptible sub-circuit is identified, logic rewriting generates several alternatives, and the candidate implementation with the lowest SER is selected. In [2, 3, 29], logic rewiring is used to evolve a design through the deletion and insertion of wires in the circuit. In essence, functionally-equivalent yet structurally-different intermediate implementations are produced, and the selection among them is driven by the objective of reducing the SER of the final implementation. Since logic rewiring has been used for several objectives in the past (e.g., area and delay minimization, testability improvement, etc.,), it provides a framework that enables the optimization of all of the design parameters, including area, power,

delay, testability, and SER. Logic rewiring, either ATPG-based [2, 29] or SPFD-based [3], enables the exploration of a different search space of functionally-equivalent designs over the use of logic rewriting techniques [12,13], as the design modifications are made globally in the circuit.

In contrast to all of the logic-level SER reduction techniques, we analyze the design trends in this work that affect the SER of the produced implementation. Thus, the analysis herein is not aimed at the reduction of SER but, rather, to provide design and test engineers an insight to the design specifications that limit the robustness of the produced logic realization of the function under synthesis, in which case alternative soft error protection techniques can be used in conjunction.

3. Soft Errors in Logic Circuits

A transient pulse, produced by a particle strike, may be tolerated within a logic circuit, if the masking factors prevent its effect from causing a soft error at the output of the design. In this section, we analyze these masking factors, and describe the designs trends that are reducing their effectiveness.

The first condition for a transient pulse to cause a soft error is that the pulse must have a path to a FF or an output of the circuit; otherwise, the pulse is *logically masked*, as illustrated using the sub-circuit example in Figure 1. Specifically, the transient pulse arriving at the top input of the AND gate (and originating from a particle strike in its fanin logic cone) would propagate to the output of the gate, since the value of its second input is logical 1 (i.e., a non-controlling value of the gate, which does not mask the pulse). Yet, the pulse is logically masked by the value of the third input in the sub-circuit (i.e., the 0 controlling value of the AND gate) and, hence, the pulse does not result in a soft error. This masking factor is independent of the technology used to design the circuit, as it depends only on the functionality and structure of the design.

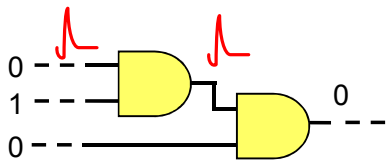

Figure 1. Example of logical masking of SETs.

The second condition for a transient pulse to cause a soft error is that the pulse must have sufficient magnitude in order to change the value of the signal; otherwise, the pulse is electrically masked, as illustrated using the sub-circuit example in Figure 2. Specifically, the transient pulse arriving at the top input of the AND gate has a small strength and, even though it propagates to the output of the AND gate, it gets attenuated by the electrical properties of the gate. Therefore, and even though the pulse now appears at the top input of the OR gate (with the other input having a non-controlling value and, hence, the pulse is not logically masked), the limited strength of the pulse does not result in changing the output value of the OR gate, and no soft error would be produced. This masking factor is dependent on the technology used to design the circuit and the operating voltage level.

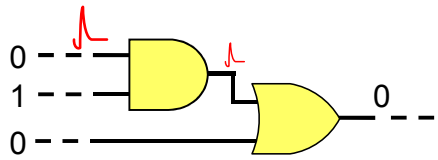

Figure 2. Example of electrical masking of SETs.

The final condition for a transient pulse to cause a soft error is that the pulse must arrive at a FF during its latching time; otherwise, the pulse is latching-window masked. In Figure 3, a positive-edge D FF is sensitive to a transient pulse at its input a if the transient pulse is active during the rising edge of the clock. In the left timing diagram, the value of a changes from 0 to 1 abruptly after the rising edge of the clock and, therefore, the FF output q is unaffected and stores the correct value of 0. In the right timing diagram, however, the pulse at input a appears during the rising edge of the clock, which causes the FF to latch the erroneous value of 1. This masking factor is dependent on the operating frequency of the design.

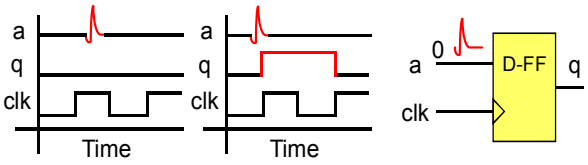

Figure 3. Example of latching-window masking of SETs.

Despite all of the above factors that may prevent a transient pulse from causing a soft error, design trends are making the SER in logic circuits unacceptable even for mainstream applications. These trends include lower voltage levels, higher operating frequencies, and reduced logic depth. In the following, we examine the effect of each one of these trends on the SER of the produced implementation.

When the operating voltage level of a circuit is reduced, the circuit becomes more sensitive to noise and transient glitches. From a SER perspective, certain pulses that are not strong enough to turn on/off transistors in higher operating voltage levels may do so in lower ones. For example, the transient pulse illustrated in the left timing diagram in Figure 4 would have no effect, as it does not exceed half of the V_{dd} value. When the voltage level is reduced as illustrated in the right timing diagram in Figure 4, the same pulse may now potentially produce a soft error, if no

masking factor results in the suppression of the pulse. In essence, this implies that the electrical masking property of logic circuits is being compromised when voltage is lowered, as more transient pulses become stronger (relative to the operating voltage level).

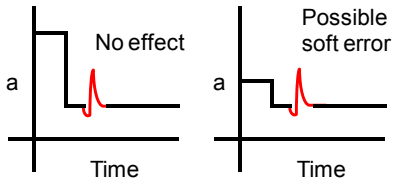

Figure 4. Effect of reducing voltage level.

Another design trend is increasing the operating frequency of logic circuits, which significantly increases the SER for the following reason. For any fixed period of time, increasing the frequency implies that there are more clock edges that latch the value at the input of FFs. Therefore, the probability that a transient pulse gets latched increases, as the latching-window masking factor is reduced. This is illustrated in Figure 5, where doubling the frequency of the clock also doubles the number of rising (and falling) edges for positive(negative)-edge FFs, making the FFs twice as vulnerable as when a slower clock is used.

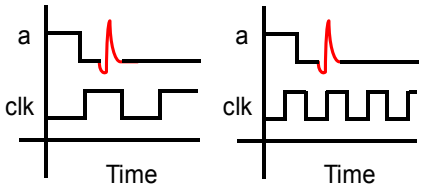

Figure 5. Effect of increasing operating frequency.

Finally, reducing the logic depth in combinational circuits, commonly performed to improve the performance of the design by limiting logic sharing, also results in increasing the SER of the implementation. This is qualitatively illustrated in Figure 6, wherein the transient pulse is highly attenuated when it propagates through more logic levels (i.e., the upper path in the figure), in comparison to when the pulse propagates through fewer levels (i.e., the lower path in the figure). Furthermore, reducing the logic depth also reduces the possibility of logical masking, as the transient pulse passes through fewer gates before reaching the output, which, in turn, reduces the likelihood that the other inputs to these gates hold a controlling value that masks the pulse.

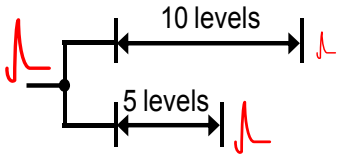

Figure 6. Effect of reducing logic depth.

4. Analysis of SER in Logic Circuits

In this section, we perform an extensive set of experiments to evaluate the soft error susceptibility and SER of logic circuits produced using different synthesis options and SER evaluation methods. First, in section 4.1, we describe the circuits and tools used in these experiments. Next, in sections 4.2 and 4.3, we evaluate the correlation between logical masking as well as the area of a circuit to its SER, respectively. Then, in sections 4.4 and 4.5, we analyze the SER dependence on the input vectors as well as the cell library used for synthesis, respectively. Finally, in section 4.6, we summarize the observations of these experiments, which pave the way for the development of synthesis-for-reliability techniques in logic circuits.

4.1. Experimental Setup

The experiments are performed using LGSynth91 [30], which is a standard set of benchmark circuits that is typically used to assess the effectiveness of various logic-circuit methods (i.e., synthesis, test, reliability analysis, etc.,). Logic synthesis is performed using the ABC [4] logic synthesis package: the circuits were optimized using Espresso [27], then mapped to the standard GENLIB library (once while it contained up to 2-input gates only, and then while it contained up to 3-input gates only). The area cost is computed using the transistor count of the produced implementation. The circuit-level SER of the circuits is computed using SERA [31], which evaluates the SER by accounting for all of the masking factors, and using HOPE [16], which accounts for logical masking only. The circuit-level SER metric is expressed using the standard number of Failures-In-Time (FIT), while the logic-level SER metric is the average number of faults detected per test pattern. In both SER evaluation methods, 500 random input vectors were applied to the circuits to evaluate their SER; the choice of using 500 vectors is justified in section 4.4.

4.2. Logical Masking and SER Correlation

In this section, we aim to illustrate the correlation between logical masking and SER, which would enable the use of fast logic-level SER assessment methods without performing intensive spice-level simulation of the transient pulses in the circuit. In order to support this correlation, we compare the SER of the circuits using SERA (i.e., circuit-level SER assessment) and HOPE (i.e., logic-level SER assessment). The SER results of the benchmark circuits are illustrated in Figures 7 and 8 as computed using SERA and HOPE, respectively. In these figures, we plot the percentile increase between the SER of the maximum susceptible input vector to the average SER of all of the simulated test vectors. We note that the curves in these figures only represent the relative

increase in the SER, and not the average SER of the circuit (which is presented in Figure 9).

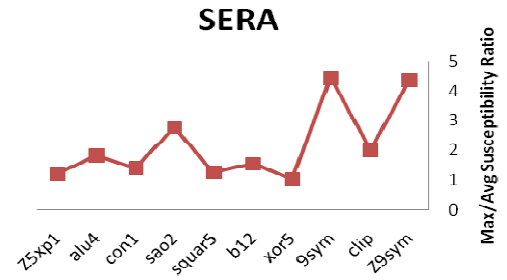

Figure 7. SERA (circuit-level) assessment of SER.

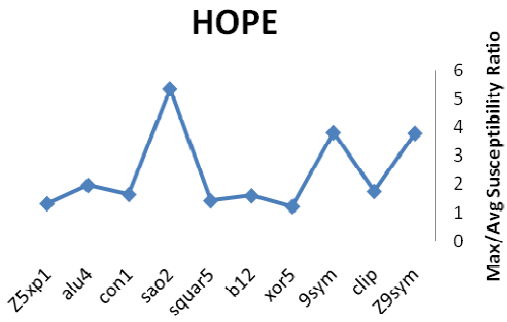

Figure 8. HOPE (Logic-Level) assessment of SER.

It is evident from Figures 7 and 8 that there is a high correlation between the logic-level and circuit-level assessment methods of SER. Therefore, the results support that the relative SER computed using logic-level SER assessment methods is also highly correlated with the actual SER of logic circuits.

4.3. Area and SER Correlation

In order to evaluate the correlation between area cost and the SER of logic circuits, we plot in Figure 9 the area cost of the optimized circuits versus the *average* SER obtained using SERA and HOPE over all of the simulated vectors.

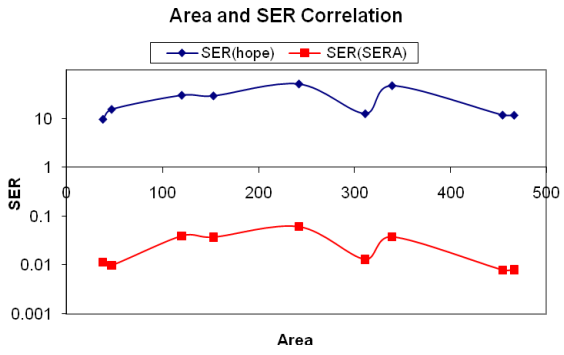

Figure 9. Area and SER correlation.

Similar to the previous experiments, the average SER computed using HOPE is highly correlated to that of SERA. Surprisingly, however, the SER is not correlated with the area of circuits. This indicates that the susceptibility of a design is dependent on its functionality, and is not simply proportional to its area size. In other words, the SER is also a function of the complexity of the implemented function as well as its area, and not necessarily the size of the area to implement such functionality. With a significant area increase, however, the SER is, typically, bound to increase as well.

4.4. SER Dependence on Input Vectors

Next, we compare the ratio between the maximum and minimum SER of the circuits, as computed by dividing the SER of the most susceptible input vector to the SER of the least susceptible input vector. This experiment illustrates the significant dependence of the SER of the circuit on the input vector being applied.

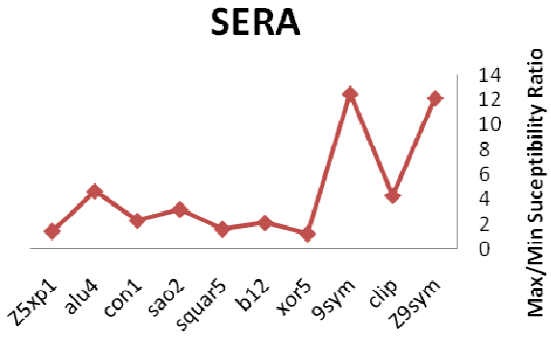

Figure 10. SER dependence on input vectors (SERA).

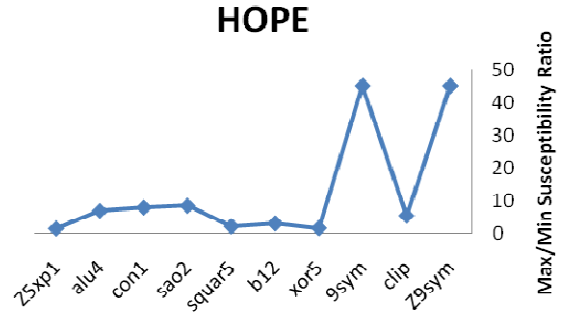

Figure 11. SER dependence on input vectors (HOPE).

The results illustrate that the SER significantly depends on the input vector. For several of the circuits, the susceptibility of the circuit increases by up to 12x (40x) in comparison to the least significant susceptible vector using SERA (HOPE). With respect to the previously-discussed masking factors, these results illustrate the significant effect of logical masking on SER, as an input vector determines the logical state of all of the internal nodes and directly impacts how many transient pulses can propagate to the output of the circuit. In other words, different input vectors sensitize different paths in the circuit and, thus, can change the probability of propagating transient pulses significantly.

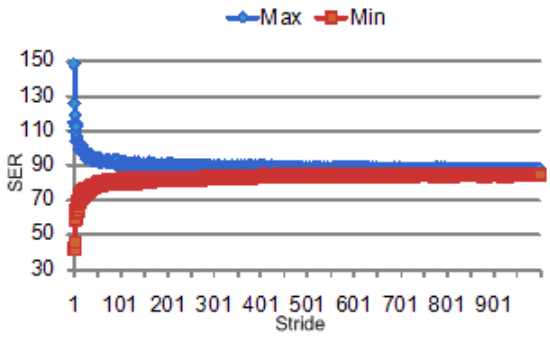

Figure 12. SER dependence on sample size (HOPE).

Finally, we illustrate in Figure 12 the maximum and minimum SER values for circuit *alu4,* as computed using *stride* input vectors. For each *stride* size, 100 randomly-generated test sets (each with *stride* test patterns) are used to compute the SER, and the maximum and minimum values are shown in the figure. As expected, the SER measure becomes more accurate as the number of test patterns used to compute SER is increased. The results indicate that using 100 test patterns to compute the SER, for example, may potentially result in a 7% deviation from the average SER value. Increasing the sample size to 500 vectors reduces the deviation to below 2.5%, while further increasing it to 1000 patterns minimally improves the accuracy to within a 2% deviation. In essence, these results indicate that the number of patterns must be large enough to ensure the accuracy of the SER metric, and that it strongly depends on the vectors in the sample; hence, application-aware SER evaluation must select the test vectors judiciously from the typical workload.

4.5. SER Dependence on Cell Library

In the final set of experiments, we evaluate the relationship between the SER and the cell library used during synthesis. Two experiments were performed: the first one by mapping the circuits to gates with up to 2-inputs, and the second one to gates with up to 3-inputs. Table 1 illustrates the average SER results for both mapping options.

Table 1. Results on LGSynth91 benchmark circuits.

Circuit Name	2- Input Gates		2/3-Input Gates	
	Average SER (SERA)	Average SER (HOPE)	Average SER (SERA)	Average SER (HOPE)
Z9sym	0.0064594	12.882	0.0077990	11.898
clip	0.0355670	50.114	0.0372292	47.526
9sym	0.0061092	13.06	0.0078764	11.82
xor5	0.0097182	15.58	0.0097182	15.58
b12	0.0367446	32.062	0.0367432	29.47
squar5	0.0372404	32.84	0.0389376	30.308
sao2	0.0123178	14.026	0.0128466	12.704
con1	0.0103644	9.696	0.0111512	9.762
alu4	0.0527284	90.602	0.0850272	85.432
Z5xp1	0.0581960	55.692	0.0600352	51.498

As can be observed, the logic-level SER (as computed by HOPE) reduces when the library includes gates with a larger number of inputs. For 9 out of the 10 synthesized circuits, the SER was either reduced or unchanged when wider gates were used. In one circuit, *con1*, the SER increases slightly by less than 1%. In contrast, the circuit-level SER assessment (as computed using SERA) illustrates an opposite trend, as the SER increases for 8 out of the 10 circuits. We caution the reader, however, that the design trends discussed in Section 3 support that logical masking will become the dominant factor in suppressing transient pulses and, hence, in computing the SER in future technologies. Therefore, the design trends support the validity of the SER trend that was observed using logic-level SER assessment (i.e., that the use of wider gates will reduce SER). Similar observations, although in the context of logic rewiring [2], also support the aforementioned conclusion.

In short, the results illustrate that the use of wider gates, which increases the probability of logical masking, results in reducing the SER of the produced implementation. Therefore, the results corroborate that the SER of logic circuits is expected to reduce if the supported library contains wider gates and/or the synthesis flow is modified to produce circuits that are composed of a larger number of wider gates than that produced in the typical synthesis flow.

4.6. Synthesis-for-Reliability of Logic Circuits

The SER of a logic circuit is dependent on the logical masking of transient pulses, area size of the implementation, input vector under application, and cell library used in mapping. Experiments were performed to evaluate the correlation between SER and these four factors, and the results support the following observations:

- Logical masking and SER correlation: logical masking is more correlated with SER than the other masking factors. Therefore, the electrical and latching-window masking factors can be excluded from the SER evaluation method, without significantly affecting the accuracy of the results.
- SER dependence on input vectors: the SER of a circuit varies significantly depending on the input vector being applied to the circuit. This is solely due to the number of paths that may propagate transient pulses occurring inside the circuit to its output, which is determined by the bit values in the input vector. Since the electrical and latching-window masking factors are unaffected by the change of input values, logical masking is the main reason behind the 10x variation of the SER of a circuit across different vectors.
- Area and SER correlation: Despite the expected high correlation between the SER and area size of

an implementation, the results illustrate that the SER is dependent on the complexity of the implemented function, as large-size circuits may have a lower SER than small-size designs.

- SER dependence on cell library: The use of wider gates when mapping logic circuits produces logic implementations that have improved resiliency to transient pulses. This may be achieved by eliminating gates with a small number of inputs from the library, or by altering the mapping step in order to favor the use of wider gates.

We note that all of the soft error mitigation methods proposed in the literature start with a synthesized netlist that realizes a specific functionality and attempt to reduce its SER. Specifically, synthesis tools are first utilized to produce an implementation of a given functional description and, subsequently, soft error mitigation methods are employed to reduce the SER of the realized implementation. Therefore, most of the soft error mitigation methods do not change the netlist under consideration in order to preserve the design parameters and optimization efforts of synthesis tools. However, the separation of the synthesis phase from the SER reduction phase may not produce an implementation with the minimal SER of the functional description, since the design space is not fully explored. This observation raises interest in the development of synthesis-for-reliability methods for logic circuits, i.e., methods that directly synthesize the implementation with the lowest SER for a given functional description through the maximization of logical masking. The synthesis of such logic circuits that implement a desired functionality with the minimum SER is part of our ongoing research.

5. Conclusions

The significant increase in the SER of logic circuits necessitates the evaluation of the correlation between design decisions and their consequent effect on the reliability of the produced implementation. In this work, we study this relationship and analyze the current design trends from a SER perspective. Furthermore, we perform an extensive set of experiments to measure the reliability of different design options, as well as investigate the variability across input patterns. Specifically, we analyze the logical masking of transient pulses, the area size of the implementation, the input vector under application, and the cell library used for mapping. While all of these parameters, collectively, dictate the SER of the implementation, our analysis suggests that logical masking will become the dominant source for improving the reliability of logic circuits. Therefore, there is a necessity to develop synthesis-for-reliability techniques that select, among the many functionally-equivalent yet structurally-different implementations of a design, the implementation with the highest logical masking of potential transient errors.

Acknowledgements

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